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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,506	05/11/2001	Mark L. Janecek	END920000132US1	6858

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EXAMINER	
ALCALA, JOSE H	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 12/04/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/853,506	MARK L. JANECEK,JOHN S. KRESGE,MARK V. P
	Examiner	Art Unit
	Jose H Alcala	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,11,12 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,11,12 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *16 September 2002* is: a)☒ approved b)☐ disapproved by the Examine

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on 9/16/02 have been approved. However, Figures 1-3 are objected, because they are improperly crosshatched. All of the parts shown in the section, and only those parts, must be crosshatched. The crosshatching patterns should be selected from those shown on page 600-81 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP 608.02.

A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7,11-14 rejected under 35 U.S.C. 102(b) as being anticipated by DiStefano et al (US Patent No. 5,640,761).

Regarding Claim 1, DiStefano teaches a three-layered laminated circuit structure, comprising: a first substrate (top substrate of Figure 2) having conductive via through holes (Reference number 26) disposed therein; and a second substrate (second

substrate from top to bottom core of Figure 2) laminated to said first substrate and having conductive, adhesive-filled via through holes (the holes that are filled with Reference number 48) that align with, and make electrical contact with, the conductive via through holes (reference number 26) of said first substrate upon lamination of said first and second substrates, and a third substrate (third substrate from top to bottom of Figure 2) laminated to said second substrate having via through holes (reference number 26) that align with, and make electrical contact with, the adhesive filled via through holes of said second substrate, thus forming said three-layered, laminated circuit structure (see Figure 3).

Regarding Claim 2, DiStefano teaches that the first and third substrates (top substrate and the third substrate from the top of Figure 4) each comprise a signal core layer (reference number 30), and said second substrate layer (reference number 42)) comprises a power core layer.

Regarding Claim 4, DiStefano teaches that said via through holes (the holes that are filled with Reference number 48) of said power core layer comprise undercut contact surfaces (column 16, lines 43-45), and said via through holes of each of said signal core layers have metallic pads (reference numbers 56a and 58a) that make electrical contact with said undercut contact surfaces of said via trough holes of said power core layer.

Regarding Claim 5, DiStefano teaches a multi-layered circuit structure, comprising: a first substrate (top substrate of Figure 2) having conductive via through holes (Reference number 20) disposed therein; and a second substrate (second

substrate from the top of Figure 4) laminated to said first substrate, and having via through holes (the hole where reference number 48 is located) comprising conductive adhesive coated pads (Reference numbers56a and 58a) that align with, and make electrical contact with, the conductive via through holes of said first substrateof the middle core, which are coated with reference number 36, which can be a conductive adhesive composite, see column 8, lines 59-62) that align with, and make electrical contact with, the conductive via through holes (Reference number 20) of said first substrate.

Regarding Claim 6, DiStefano teaches that said first substrate (top substrate of Figure 2) comprises a signal core layer (reference number 30), and said second substrate (second substrate from the top of Figure 2) comprises a power core.

Regarding Claim 7, DiStefano teaches further comprising a third substrate (the third substrate from the top of figure 2) having similar structure to that of said first substrate (See Figure 2, where both substrates are "similar"), said first and third substrates each being laminated to said second substrate (See figure 3), and wherein said first and third substrates each define a signal core layer (reference number 30), said second substrate further defining an inner power core layer (reference number 42) sandwiched between each of said signal core layers (See Figures 2 and 3).

Regarding Claim 11, DiStefano teaches a multi-layered circuit structure, comprising: first (top substrate of Figure 2) and second (third substrate from the top of Figure 2) substrates, each having conductive via through holes (Reference numbers 26) disposed therein; and a third substrate (second substrate from the top of Figure 2)

laminated between said first and second substrates and having conductive, adhesive filled via through holes (the hole where reference number 48 is located) that align with, and make electrical contact with, the conductive via through holes of said first and second substrates (See Figure 3).

Regarding Claim 12, DiStefano teaches that said first (top substrate of Figure 2) and second (third substrate from the top of Figure 2) substrates comprise a signal core layer (reference number 30), and said third substrate comprises a power core layer (reference number 42).

Regarding Claim 14, DiStefano teaches that said via through holes (the holes that are filled with Reference number 48) of said inner power core layer comprise undercut contact surfaces (column 16, lines 43-45), and said via through holes of each of said signal core layers have metallic pads (reference numbers 56a and 58a) that make electrical contact with said undercut contact surfaces of said via trough holes of said power core layer.

Response to Arguments

4. Applicant's arguments with respect to claims 1-2,4-7,11-12 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jose H Alcala whose telephone number is (703) 305-9844. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3431 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JHA
December 2, 2002

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800